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Trans-Admittance Trans-Impedance Logic for Integrated Circuits

Cross-References to Related Applications

This application is a continuation-in-part of U.S. Serial No. 09/746,989, filed on December 22, 2000, patent number which is a continuation-in-part of U.S. Serial No. 09/415,602, filed on October 8, 1999, both applications are herein incorporated by reference in their entirety. patent number 6297706

Field of the Invention

The present invention relates to an improved integrated circuit, and in particular, to an integrated circuit that enhances the performance of logic gates when operating at the limits of the transistor bandwidth.

Description of Related Art

Figure 1 is a conventional logic gate 100, such as an emitter-coupled logic (ECL) or current-mode-logic (CCL) integrated circuit, that may be cascaded in a chain. This conventional logic block receives input voltage signals and produces output voltage signals. Each logic gate includes a current switching stage or clocked trans-admittance stage (TAS) 110 comprising transistors T1, T2, T3, T4, T5, T6; a passive load resistance 120 comprising resistors R1, R2; and two emitter follower transistors T7, T8 that buffer the wire/fan-out capacitance driven by the logic gate and provide level-shifting. This conventional logic gate is disadvantageous in that the use of a passive load 120 does not produce enough gain at the

limit of transistor bandwidth, e.g., gain greater than one. At multi-GHz frequencies the wires have significant transit delay (time of flight). The impedance mismatch between the line impedance and the emitter-follower results in multiple reflections that degrade the signal at the input of the next logic gate. To reduce or eliminate impedance mismatch wires are implemented on the collectors of the transistors T3, T4, T5, T6. The resistance times the line capacitance from the wires on the collector nodes of the transistors reduces the peak clock frequency.

It is therefore desirable to develop a logic gate that is better suited for signal routing and less sensitive to capacitance from wiring while providing more gain at a higher bandwidth.

Summary of the Invention

The present invention is directed to a logic circuit that solves the aforementioned problems.

In particular, the invention relates to a latch including a clocked trans-admittance stage circuit for receiving a voltage and producing a current output, and an active load, such as a trans-impedance stage circuit, connected to receive as input the current output of the trans-admittance stage circuit and produce a voltage output.

The invention is also directed to a cascaded latch chain including a clocked trans-admittance stage latch receiving an input voltage and producing an output current. In a further embodiment, the latch chain may also include a trans-impedance circuit and one or more latch pairs, with each pair having two independent trans-admittance and trans-impedance stages.

Yet another aspect of the invention relates to a latch pair including two independent combined trans-admittance and trans-impedance stages, with each latch pair clocked to opposite phases of a clock signal.

Brief Description of the Drawings

The foregoing and other features of the present invention will be more readily apparent from the following detailed description and drawings of illustrative embodiments of

the invention wherein like reference numbers refer to similar elements throughout the several views and in which:

Figure 1 is a prior art logic gate circuit;

Figure 2a is an exemplary TAS latch;

Figure 2b is an exemplary RL - TAS latch;

Figure 2c is a logic gate symbol for an exemplary cascaded chain comprising a TAS latch and two RL - TAS latches;

Figure 3a is an exemplary single stage TAS - TIS latch;

Figure 3b is an exemplary TAS - TIS latch pair comprising two independent TAS - TIS stages;

Figure 3c is a logic gate symbol for the TAS- TIS latch pair of Figure 3b;

Figure 4a is a clocked TAS latch;

Figure 4b is a logic gate symbol for the clocked TAS latch of Figure 4a; and

Figures 5a-5c are exemplary functional blocks with logic gates in accordance with the present invention.

Detailed Description of the Invention

To increase the gain of a conventional logic circuit the passive load resistance 120 in Figure 1 may be replaced with an active load resistance, such as a trans-impedance stage. An active load resistance provides more gain at a higher bandwidth. A digital circuit comprising several conventional digital gates as shown in Figure 1 is divided into blocks and regrouped to provide current rather than voltage interfaces at the inputs and outputs. Current interfaces are better suited for signal routing as the capacitance on the signal lines has minor impact on circuit speed and does not degrade circuit stability. In particular, the digital circuit is divided into a latch chain comprising a TAS latch connected in series to one or more RL - TAS latches. Figure 2a is a circuit diagram of the TAS latch formed by transistors T1, T2, T3, T4 that receives clocked signals (e.g., clock (clk) and clock bar (clkb)), an input voltage Vin, Vinb and produces an output current Iout, Ioub. The circuit diagram for the RL - TAS latch, as shown in Figure 2b, comprises an RL passive resistance load block of resistors R1, R2 and the TAS block formed by transistors T1, T2, T3, T4, T5, T6. Also included in the RL

- TAS latch are emitter followers T7, T8. The RL -TAS latch receives a current input Iin, Iinb from the first TAS latch in the chain and produces a current output Iout, Ioutb.

A chain may be formed by cascading a series of RL - TAS latches clocked on opposite phases of the system clock. Figure 2c is an exemplary symbol diagram of a cascaded latch chain in accordance with the present invention. The first TAS latch in the chain receives an input voltage Vin, Vinb and produces a current output Iout, Ioutb. By way of example, the chain in Figure 2c has two RL - TAS latches, however, any number of one or more RL - TAS latches may be cascaded together, as desired. Each RL - TAS latch receives a current Iin1, Iin1b and produces a current output Iout1, Iout1b.

Sub B1

In accordance with the present invention, the load resistors in the RL - TAS latch, shown in Figure 2b, can be replaced with an active resistance load, for example, a trans-impedance amplifier stage (TIS). Figure 3a is a TAS - TIS latch in which the passive load resistance RL comprising R1, R2 has been replaced with an active TIS load including transistors T9, T10, T11, T12 and resistors R3, R4, R5, R6. The TIS load converts an input current to an output voltage.

Sub A1

Logic gates configured in accordance with the present invention are less sensitive to transistor collector capacitance and/or wiring capacitance on the collectors of the transistors T3, T4, T5, T6. In addition, the topology shown in Figure 3a provides a convenient node in the circuit that can be used for input/output connections between logic gates. Specifically, logic gates in accordance with the present invention are arranged to have a TIS input stage and a TAS output stage. Thus, the current from the switched TAS output is received by the TIS input stage of the next logic block in the cascaded logic chain.

A gain greater than one is required in order to propagate a digital signal along a chain of logic gates. The TAS-TIS logic gate in accordance with the present invention provides more differential gain than conventional logic gates operating at maximum frequency. In addition, the bandwidth or corner frequency for gain roll-off is extended by the TAS-TIS logic gate relative to that achieved using conventional logic gates. The TAS-TIS logic gate also provides more common-mode rejection between gates than with conventional logic gates. Improved noise or spurious signal rejection may also be obtained using the TAS-

TIS logic gate construction. This characteristic is particularly advantageous at relatively high frequency where noise or spurious signals may be coupled into the circuit.

For efficient use of power and area two independent TAS -TIS stages may be grouped in the same block. Figure 3b shows a latch pair comprising two independent TAS - TIS stages, wherein the two stages are clocked on opposite phases of a clock signal clk (clock) and clkb (clock bar). Figure 3c is a digital logic circuit symbol of the two stage TAS - TIS latch pair.

Figure 4a is a two stage clocked TAS latch in accordance with the invention which receives an input voltage Vin1, Vin1b, Vin2, Vin2b and produces an output current Iout1, Iout1b, Iou2, Iout2b. Transmission lines TL 1, TL2, TL3, TL4 may be coupled between the outputs of the TAS circuit and the inputs of the TIS circuit. The nominal frequency range of oscillation of the overall circuit may be adjusted by selecting the length of the transmission lines TL 1, TL2, TL3, TL4. A clock signal acts as a selector between Vin1, Vin2. In particular, when the clock signal (clk) is active, the input voltage Vin1, Vin1b is output as current Iout1, Iout1b, whereas when clock bar signal (clkb) is active, the input voltage Vin2, Vin2b is output as Iout2, Iout2b. The logic gate symbol of the two stage clocked TAS latch is shown in Figure 4b.

The modified logic gates in accordance with the present invention have a wide range of functional applications. By way of example, in Figure 5a, a clocked TAS latch is coupled with a TIS latch to form a two-in-one selector for voltages. The clocked TAS latch selectively receives two input voltages Vin1 and Vin2 and produces output current Iout1, Iout1b, Iout2, Iout2b. The TIS latch selectively receives as a current input Iin, Iinb from the output current Iout1, Iout1b, Iout2, Iout2b of the clocked TAS and produces a single voltage output Vout1, Voutb.. In another exemplary application of the logic gates in accordance with the present invention, Figure 5b shows a two-to-one multiplexer of a cascaded chain comprising a clocked TAS, two TAS - TIS latch pairs and a TIS latch, while Figure 5c shows the reverse processing of a one-to-two demultiplexer. Other functional applications of the logic circuit in accordance with the present invention are contemplated and within the intended scope of the invention.

The logic gate in accordance with the present invention provides more gain at higher bandwidth than conventional logic gates. Line impedance and TIS input impedance are selected to minimize reflections and adsorb the line capacitance, thereby increasing the peak clock frequency.

Thus, while there have been shown, described, and pointed out fundamental novel features of the invention as applied to a preferred embodiment thereof, it will be understood that various omissions, substitutions, and changes in the form and details of the devices illustrated, and in their operation, may be made by those skilled in the art without departing from the spirit and scope of the invention. For example, it is expressly intended that all combinations of those elements and/or steps which perform substantially the same function, in substantially the same way, to achieve the same results are within the scope of the invention. Substitutions of elements from one described embodiment to another are also fully intended and contemplated. It is also to be understood that the drawings are not necessarily drawn to scale, but that they are merely conceptual in nature. It is the intention, therefore, to be limited only as indicated by the scope of the claims appended hereto.